University of Arizona
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Rev. 3.0

I/O Specification for Serial Transmitter Daughter Board (PCB-0140-XMIT)

(Revised July 7, 1999)

1.0 Introduction

The Serial Transmitter Daughter Board accepts 16 bit parallel data at rates from 47.8 MHz to 58.4 MHz and creates a serial data stream at 20 times the parallel word rate that is 8b/10b encoded.

The Serial Transmitter Daughter Board is manufactured in 2 versions, one that uses 3.3V only and another that uses both 3.3V and 5V. The 2 versions are completely compatible and can be used interchangeably, provided that the 5V pin on the connector is powered.

This document is intended to explain the electrical and physical requirements for using this board.

2.0 Inputs and Outputs

The following sections describe the I/O connectors on the Serial Daughter Board.

2.1 Parallel Inputs

The parallel data is input through a 30 pin connector (Samtec P/N TFM-115-02-S-D-LC), all inputs are compatible with both 3.3v and 5v logic inputs. The Inputs are shown in Table 1. Word_Clock is a free-running clock at the RF frequency and all other inputs, including Enable, are referenced to this clock. The input levels are compatible with either 5V or 3.3V logic families, depending on how power is applied to the connector. Pin 27 can be connected to either 3.3V or 5V to set the input voltage levels.

All inputs have a setup time (t_{su}) of 8ns with respect to the rising edge of Word_Clock and a hold time (t_h) of 2ns with respect to Word_Clock. The board transmits the Fibre Channel SYNC character (K28.5) when the Enable signal is low, encoded data when the Enable Signal is high and even longitudinal parity when both the Enable Signal and Parity_Enable signals are high (see Figure 1). Parity_Enable causes even longitudinal parity, calculated starting from the last Parity_Enable or Enable signal, to be transmitted in place of data. The parity word is typically added as the seventh word after the six data words sent for a bunch crossing, but can be added over any length of words at the discretion of the user. Serial Data will start appearing at the serial output 4 clock cycles after it is input to the board.

2.2 FAST-OR Output

The FAST-OR Output, which is compatible with both 3.3V and 5V logic levels, goes true whenever any of the parallel data inputs is high and stays true for the rest for that bunch crossing.

2.3 JTAG/Programming Connector

A 10 pin connector (Samtec P/N TFM-105-02-S-D-A) is provided for those users who wish to use the JTAG Boundary Scan Test capabilities of the Altera EPLD that drives the output lines of the Serial Transmitter Daughter Board or to use the JTAG connector to reprogram the Altera EPLD. Users that do not wish to reprogram the Serial Transmitter card in system can ignore this connector. Table 2 shows the pin assignments for this connector.

Table 1 - Parallel Inputs

Pin #	Label	Description
1	GND	Ground
2	GND	Ground
3	Data_In_0	LSB of Input Data
4	Data_In_1	Input Data
5	Data_In_2	"
6	Data_In_3	"
7	Data_In_4	"
8	Data_In_5	"
9	Data_In_6	"
10	Data_In_7	"
11	Data_In_8	"
12	Data_In_9	"
13	Data_In_10	"
14	Data_In_11	"
15	Data_In _12	"
16	Data_In_13	"
17	Data_In_14	"
18	Data_In_15	MSB of Input Data
19	Fast_OR	Fast Or Output
20	Word_Clock	RF Clock
21	Enable	High = Data Enabled
22	Parity_Enable	High = Transmit Parity
23	Spare	
24	GND	Ground
25	+5V	+5 volt Power Supply
26	+5V	+5 volt Power Supply
27	+3.3V or +5v	Output Power Supply
28	GND	Ground
29	+3.3V	+3.3 volt Power Supply
30	+3.3V	+3.3 volt Power Supply

Table 2 - JTAG Connections

Pin #	Label	Description
1	TCK	Test Clock In
2	GND	Ground
3	TDO	Test Data Out
4	Vcc	+5v
5	TMS	Test Mode Select
6	NC	
7	NC	
8	NC	
9	TDI	Test Data In
10	GND	Ground

2.4 Serial Outputs

There are two identical Serial Data Outputs on the Serial Transmitter Daughter Board, although usually only one of them is installed on the board.

3.0 Timing Requirements

Figure 1 shows the relationship between the Input Data, Parity_Enable and the clock. Words 1 to 6 contain the data for the bunch crossing and word 7 will contain the parity word that is generated on the Serial Transmitter Daughter Board. Note that the Serial Transmitter Daughter Board will generate odd parity for all the words since the last Parity_Enable signal, so it is possible to generate parity of messages of any length.

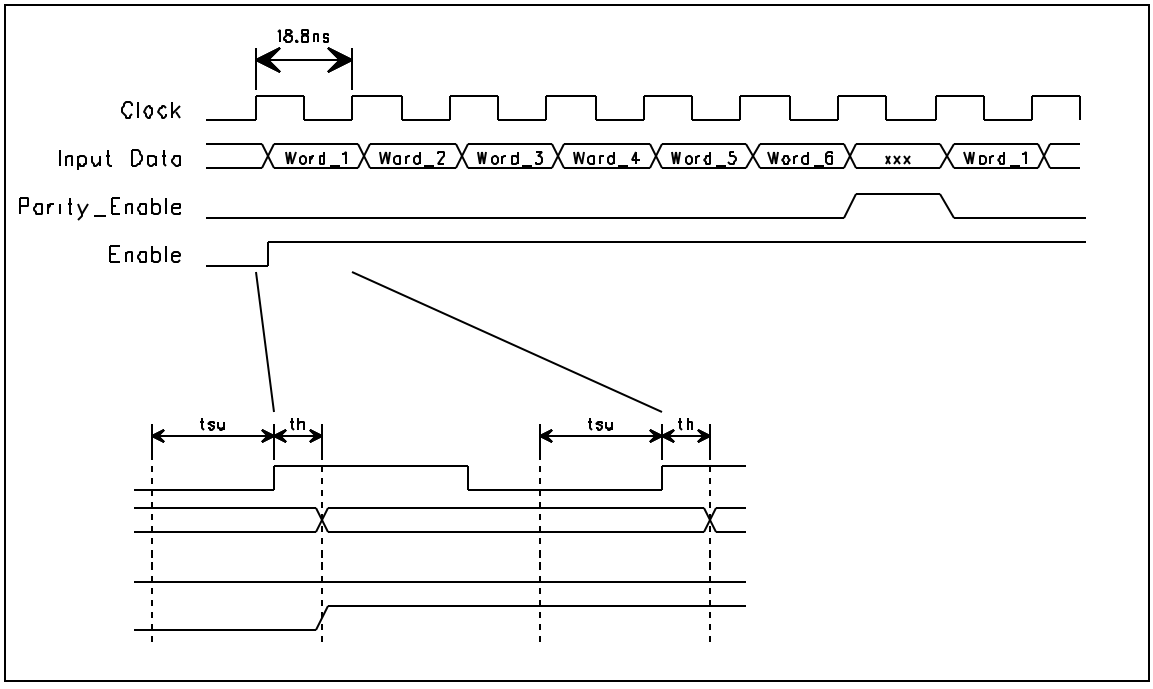


Figure 1 - Input Timing

4.0 Mechanical Layout

The Serial Transmitter Daughter Board is 1.5” x 2.2” and has 4 mounting holes as well as the connectors that attach to the daughter board. Figure 2 shows the mechanical arrangement of the board.

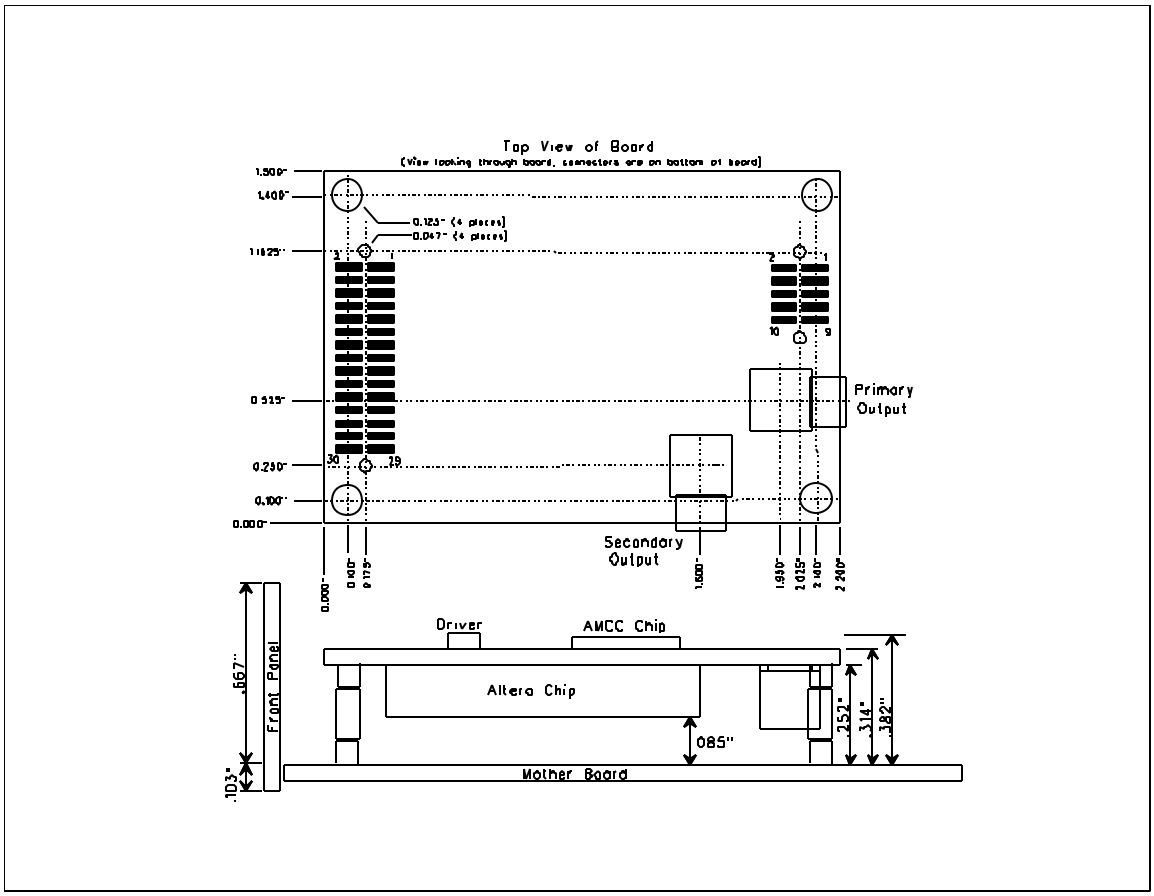
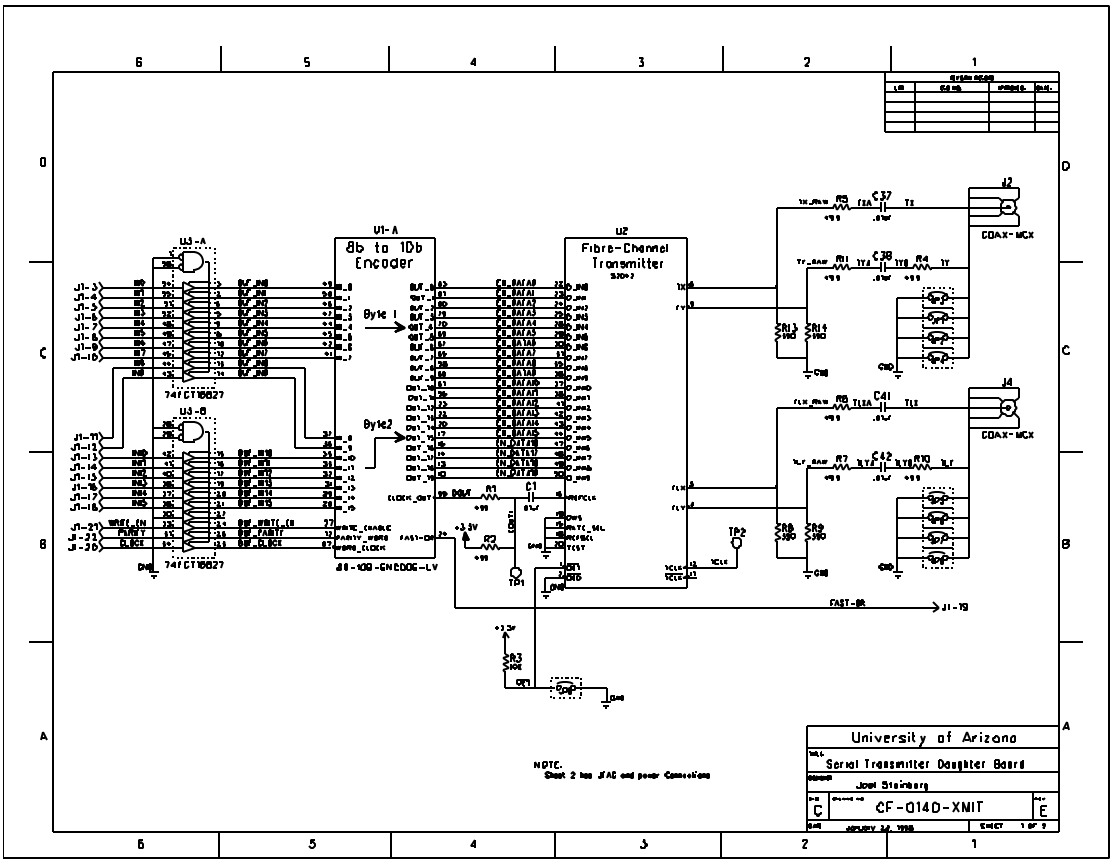
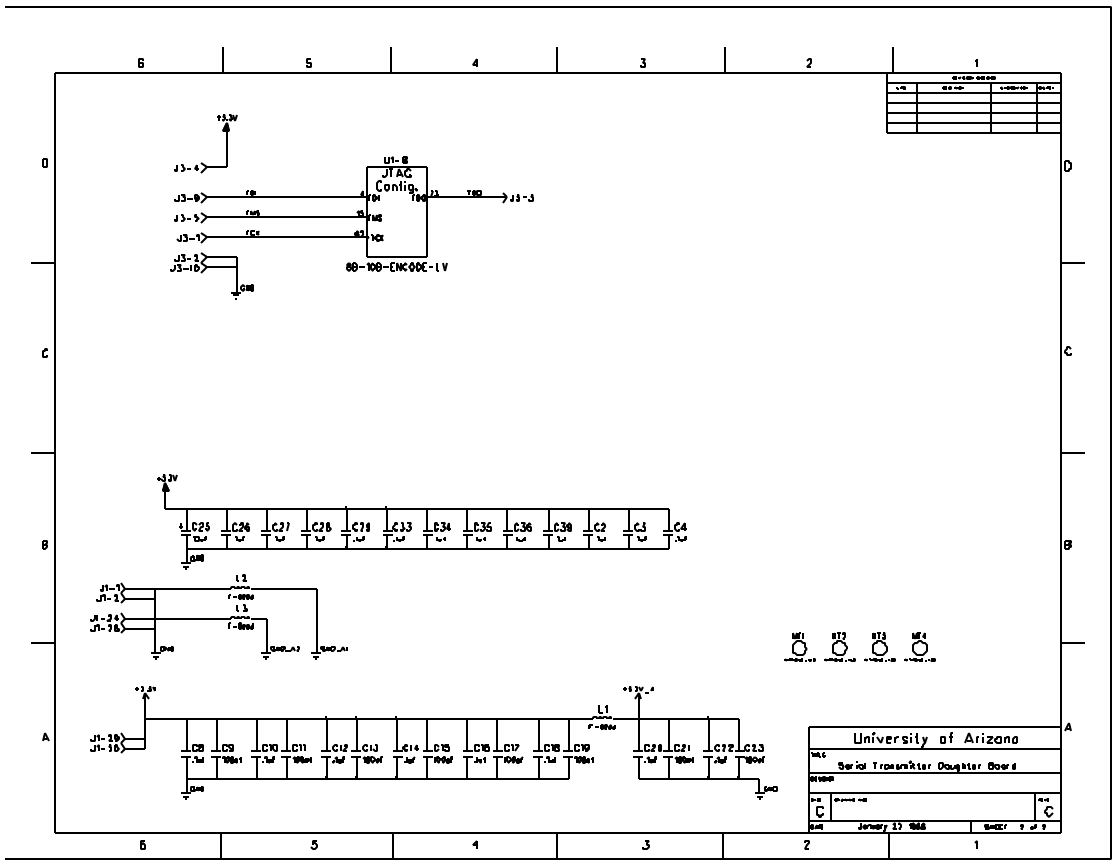


Figure 2 - Mechanical Layout

Appendix A - Board Schematic




JTAG
Config.
68-100-ENC00E-1V
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Serial Transmitter Daughter Board